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Design and Implementation of an Interfacing Technique Between The Microcomputer and A Three-Phase Induction Motor Control System

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Abstract

The speed of a three-phase induction motor can be varied within a wide range other than its rated value if its input parameters are varied properly. For industrial and some other sophisticated use of three-phase induction motor, precise and accurate control of the speed of the motor is necessary. Introduction of microcomputer and associate of software programs in three-phase induction motor control system as proposed is accurate and reliable in terms of accurate and complex speed control of the motor. In the present work an interfacing circuit, and associated software program is designed, developed and implemented through which microcomputer can read motor speed and can write codes to the control circuit to set the motor speed. Interfacing circuit is connected to the IBM microcomputer through I/O slot and program is written in C language. Transistorized infrared opto coupler is used to sense the motor speed in the place of conventional techo generator yielding faster and more accurate speed sensing capability. During the write action accurate input voltage is set for Voltege Controlled Oscillator(VCO) through D/A converter and motor input voltage is set via digitally controlled AVR.

KEYWORDS: Motor, Drive, Interface, VCO, Computer

1. INTRODUCTION

In this paper attempts are made to explain in detail what has been designed and developed in terms of hardware and software for establishing successful and reliable interfacing between the microcomputer and control circuit[1,4,5,6,7,8]. Obviously the whole work has been divided into two major sections. They are

a) Design and development of electronics circuit

b) Design and development of software programs

Obviously the success of the present interfacing relies on the successful coordination of hardware and software operation.

2. COMPUTER INTERFACING CARD

To establish data communication between microcomputer and motor control circuits we developed an electronic circuit. We call this circuit board as computer interfacing card because it performs the equivalent service as conventional cards do. Fig. 1 is the circuit diagram of the computer interfacing card. The circuits of this interfacing card is divided into three main sections. They are:

a) Address decoding section[1,2,8,12,13]

b) Data reading section[1,8,9,10,11,12]

c) Data writing section[1,8,9,10,11,12]

To establish physical connection between I/O slot of microcomputer[1,8,12,13] and interfacing card we used a 24 wire parallel bus. Among them 10 wires have been used for address, 8 wire for data, 2 wire for Read/write, 1 for address enable, 1 for system clock, 1 for ground, 1 for +5V.

2.1 Address Decoding section

This section comprises of one magnitude comparator (74LS688), one demultiplexer (74LS138) and one NAND Gate (7403)[Fig. 1]. A brief discussion of the above chips are given below.

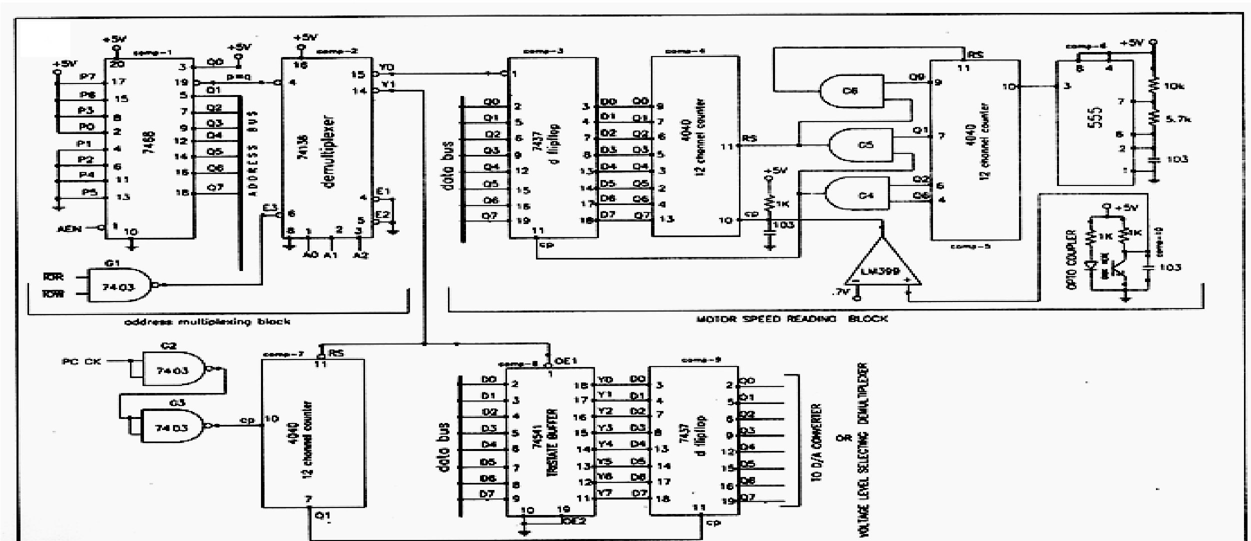
74LS688 is a magnitude comparator. It can also be used as a programmable decoder. It is a 20 pin DIP IC. It performs comparison between two eight bit binary or BCD words. Pins 3, 5, 7, 9, 12, 14 and 18 (Q0-Q7) are address inputs and pins 2,4, 6, 8, 11, 13, 15 and 17 (P0-P7) pins are programmed for a desired address. Its output pin 19 will be active (low) only when that desired address appears at the address inputs (Q0-Q7).

A 3 to 8 line decoder/demultiplexer(74LS138) is used and its output becomes active (low) when a specific (1 of 8) memory address is chosen. A Quad 2 input NAND gate(74LS03) is used for Read, write mode selection

In our present design we can select 8 addresses (320H-327H) though we are using only two. The bit patterns of the address 320H, 321H are given below.

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	1	0	0	0	0	0	= 320H
1	1	0	0	1	0	0	0	0	1	= 321H
P7	P6	P5	P4	P3	P2	P1				
Q7	Q6	Q5	Q4	Q3	Q2	Q1				

Po = Qo = +5V



Computer interfacing circuit

Fig. 1 , Different Section of Computer Interfacing Circuit

To ensure the above bit patterns, wires A0, A1, and A2 of address bus are connected to the encoding inputs(1,2 and 3) of demultiplexer 74LS138. P0 and Q0 of magnitude comparator 74LS688 are connected to high. Pin P1 to P7 are programmed as per pattern. Q1-Q7 are connected properly to the address bus. Read and write wire are connected to the two inputs of a NAND gates and the output to the NAND gate is connected to the enable pin 6 of the decoder 74LS138. As a result when address 320H and Read /Write action prevails in the bus, Y0 (pin 15) of 74LS138 is active(low), which we use for reading action. Similarly when address 321H and Read/Write action prevails in the bus, Y1(pin 14) of 74LS138 becomes active(low), which we use for write action.

2.2 Data Reading Section

This section comprises of one D-flipflop (74LS37), two counters(4040), three NAND-gates, 3 AND gates one triple five timer(555), and one optocoupler.[1,8]

Working Procedure: A U shaped infrared optocuopler (component-10 in Fig. 1:) is used to count motor speed. A circular disk with 8 slits along its circumference is attached to the rotor of the three-phase motor. The opto coupler is loaded on a stand in such a way that the disk can move between the two wings of the opto coupler when the rotor of the motor moves.

When the open portion of the disk stands before the base of the transistor, infrared from the diode falls on the base of the transistor, the transistor conducts and the collector (10p) of the transistor goes low. But when the opaque portion of the disk stands

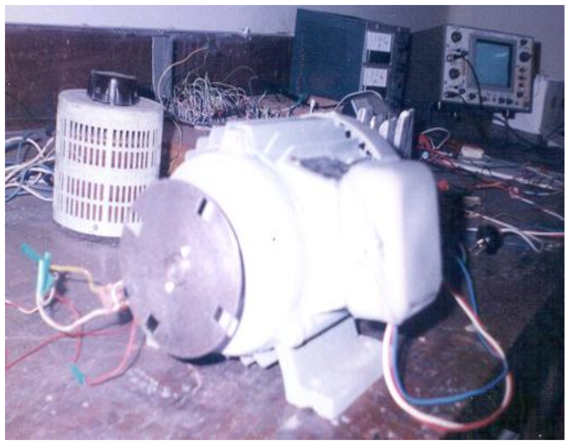


Fig 2 , Pulse generation (Disk, opto coupler & motor)

Fig 2.1, Pulse generated from opto coupler

before the base of the transistor, no infrared falls on the base of the transistor, it does not conduct and the collector (10pl) goes high. As a result when one slit of the disk passes between the two wings of the optocoupler, a pulse in generated at the collector of the transistor(Fig. 2). So, one revolution of the disk, i.e. one revolution of the motor rotor generates 8 pulses. These pulse are further shaped with the help of a comparator LM399 and then fed to the input of the counter 4040 (comp-4).

Simultaneously 200 HZ pulse is generated with the help of a 555 timer. These pulse are fed to the counter 4040(comp-5) at pin 10. When this counter counts 68, Q6 and Q2 of comp_5 are high, the output of AND gate(G4) goes high which generates an up going pulse at pin 11 of D-flip-flop(comp-3) and instantly the output count of comp-4 is stored in the internal buffer of D-flip-flop(comp-3). When the counter(comp-5) counts 70; Q6, Q2 and Q1 are high; output of gate

G5 goes high and resets the counter(comp-4). When 71 is count, Q6, Q2, Q1 and Q0 goes high and output of gate G6 goes high and instantly resets itself. All the count pins (Q0-Q11) go low and counters(comp-4, comp-6) and D-flip-flop(comp-3) become active again. Counting process repeats in this way at the interval of every 71 pulses time duration but the count stored in the internal buffer of D-flip-flop(comp-3) is 68 pulse duration time.

When address 320H is selected by the microcomputer, Y0 of comp-2 and pin 1 of comp-3 go low. When pin 1 of comp-3 is low, the data in the internal buffer of comp-3 is transparent to the data bus. So setting address 320H in the read mode microcomputer reads the count(Data) and after further calculation the computer displays the motor speed on the monitor.

Calculations :

Frequency at the input of counter(comp-5) = 200 Hz

Pulse width = 1/200 Hz = 5 ms

So, sampling time = duration of 68 pulses

$= 5 \times 10^{-3} \times 68 \text{ sec} = 340 \times 10^{-3} \text{ sec}$

Let count stored at the internal buffer of comp-3 is **N**, which is generated from the optocoupler due to the disk's rotation.

Therefore,

pulses generated per second = $(N / 340 \times 10^{-3})$

Rotor rotation per second = $(N /(8 \times 340 \times 10^{-3}))$; *8 is the No. of slots per disk*

Motor speed = $(N \times 60) /(8 \times 340 \times 10^{-3})$ rpm

$= 22.05$ N rpm

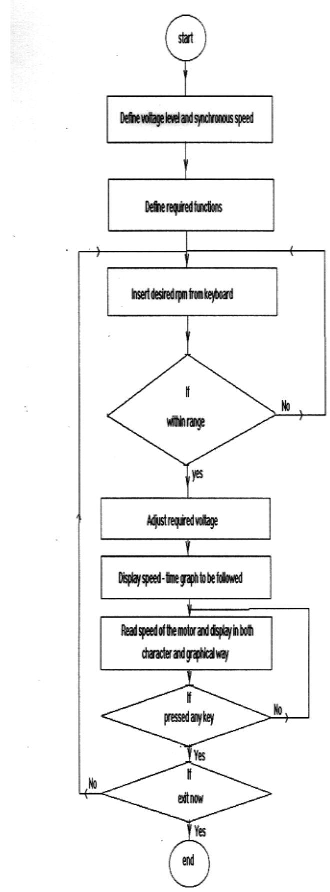


Fig 3 (a), Flow chart of software

2.3 Data writing Section

This section consists of one counter 4040 (comp-6) one tristate buffer 74541, (comp-8), One D-flip-flop 7437, (comp_9), and two AND gates.

The working procedure: When micro computer selects/decodes address 321H at a writing mode, Y1 of comp-2 goes low. This enables tristate buffer comp-8. So, data in the data bus is available at the input of D-flip-flop, i.e. comp-9. Again due to the low level of Y1 as well as reset pin 11 (Rs) of counter (comp-7), it becomes countable. Clock pulses from microcomputer are always available at the input of this counter(comp-7) through NAND gates G2 and G3. As soon as the counter(comp-7) becomes countable due to the low stage of Y1, clock pulse are available at pin 7 of comp-7. These pulses are fed at pin 11 of comp-9 which transfers the data at its input (Do-D7) to the output (Q0-Q7) and remains same until further change. So, instructed by the program, computer writes eight bit data at the output of comp-9. This data is further decoded to select an appropriate voltage level to drive VCO for generating inverter frequency.

3. THE SOFTWARE

To establish a successful and efficient communication between the microcomputer and the motor control circuit, it needed to write plenty of programs to perform and control a number of activities in real time mode. We had to choose a software to write the required programs which would be able to provide the following facilities:

a) efficient computing speed and accuracy

b) embedding assembly language command in the program to perform chip/register level communication.

c) capable of handling graphics display to render visual impression.

d) capable of dividing the big task into small modules and accumulating them under a main program.

In order to fulfill all these requirements C software was chosen as the programming language.[9,10,11]

Working steps of the Program as coded in C language:

The flow chart is shown in Fig.3.a. The whole motor speed range is devided into several steps and associated VCO voltage level, and inverter voltage is pre declared. Inserting required values and clicking run button as shown in Fig 3.b motor begins to start.

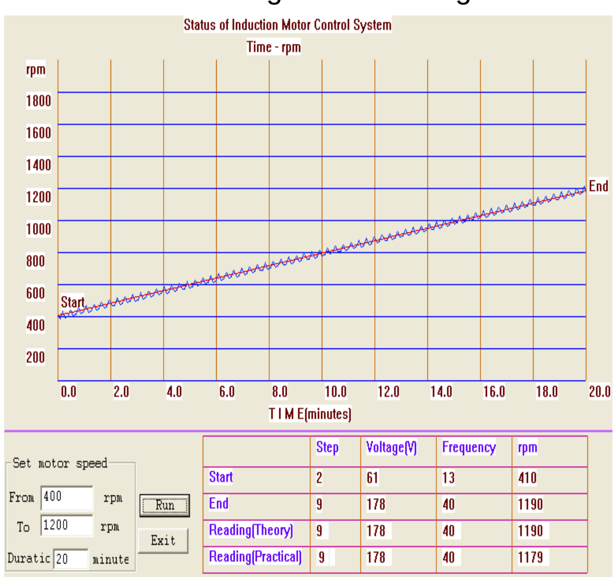


Fig 3 (b), Computer screen

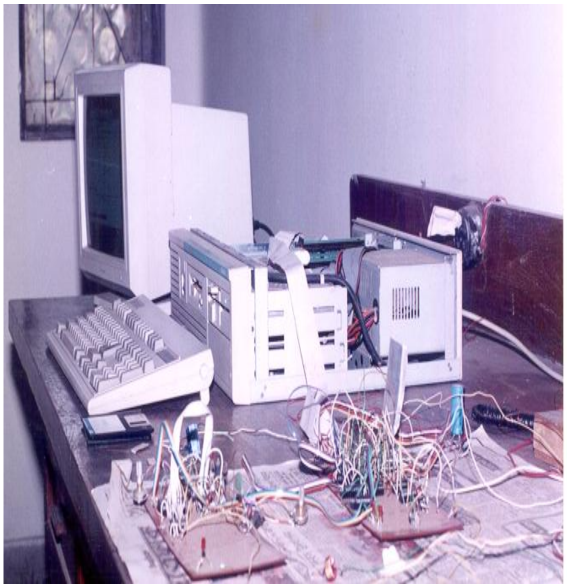


Fig 3 (c), Computer interfacing with inverter

To write 0 level at address 0321H following assembly language is used.

```
-AL = 0;                 // loads the lower eight bit of Accumulator with zero
 asm MOV DX, 0321H;      //Loads 0321H in DX register
 asm OUT DX, AL;         // weites the content of AL register to 0321H address
```

CONCLUSION

In the present work with the help of proper electronics circuit and software program a successful interfacing is established between an IBM microcomputer and a motor control circuit. Data communication to and from IBM micro computer is performed through I/O slot But this I/O slot is situated within the computer. To make interfacing through I/O slot we need to open the cover and keep the computer uncovered till the end of the work. This situation is seen in Fig. 3.c. Again as all the pins of I/O slot bear only +5V and 0V signal, we can not use a long wire bus to make that kind of communication due to the attenuation problem. So, the Computer, the control circuit, the inverter and the motor all should be kept close together which should be on the same table as we did during the whole work. But this is not logical to keep the computer close to the motor and control circuit. If we use some signal amplifier and serial port communication between the computer and control circuit, we can keep the computer away from the control circuit and the motor. In that case it would be needed to change both software program and circuits of interfacing card to establish such a serial Port communication.

FUTURE WORK

In order to control numbers of induction motors from the same computer both software algorithm and interfacing circuit should be improved. More dedication more work deserves this but it is hoped that then the improved version will widely used in the industry.

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