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Carrier Conduction Time Delay Model in Subthreshold Regime of Pocket Implanted Nano Scale n-MOSFET

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Abstract

In this paper, an analytical carrier conduction time delay model in subthreshold regime of the symmetric pocket implanted nano-scaled n-MOSFET has been presented. The model is developed using the inversion layer charge and subthreshold drain current model for pocket implanted n-MOSFET. The model incorporates the linear pocket profiles symmetric both at the source and drain sides. The linear profiles are then converted into the effective doping concentration by mathematical integration along the channel. Electron current density per unit area is obtained from the conventional drift-diffusion equation in the subthreshold regime. Then inversion channel charge density per unit area is calculated for the pocket doped channel. Thus conduction time delay is found in the subthreshold regime. The simulation is carried out for different pocket profile and device parameters as well as for various bias voltages. The results show that the derived model can produce the conduction delay time in subthreshold regime that can be utilized to study and characterize the pocket implanted advanced ULSI devices.

Keywords: Pocket Implantation, n-MOSFET, Conduction Time Delay, Subthreshold Regime.

1. INTRODUCTION

As the channel length of MOSFETs is scaled down to deep-submicrometer or sub-100 nm regime, we observe the reduction of threshold voltage with the reduction of channel length due to the charge sharing between the drain/source region and the channel [1]. Also, the off-state leakage current increases due to sensitivity of the source/channel barrier to the drain potential or drain induced barrier lowering (DIBL). This effect is known as short-channel effect (SCE). This effect arises as a result of two dimensional potential distribution and high electric fields in the channel region [2]. It can be reduced or can even be reversed (then it is called reverse short channel effect or RSCE in short) by locally raising the channel doping near source and drain junctions. Lateral channel engineering utilizing halo or pocket implant [3-7] surrounding drain and source regions is effective in suppressing SCE. The halo or pocket implant can be either symmetrical [8] or asymmetrical [9] with respect to source or drain. Reported circuit applications include a 256 M-bit DRAM [10] and mixed-signal processor [11]. In fact, this pocket implant technology is found to be very promising in the effort to tailor the short-channel performances.

When the gate voltage is below the threshold voltage and the semiconductor surface is in weak inversion, the corresponding drain current is called the subthreshold current. The subthreshold region is particularly important for low-voltage, low-power applications, such as, when the MOSFET is used as a switch in digital logic and memory applications, because the subthreshold region describes how the switch turns on and off. Already few papers have been published focusing on the subthreshold behaviour of pocket implanted MOSFET [12-14]. In [7], models for subthreshold and above subthreshold currents in 0.1 m pocket n-MOSFETs for low-voltage applications have been derived based on the diffusion current transport equation using step profile. An analytical subthreshold current model for pocket-implanted n-MOSFETs has been presented in [14] also using step pocket profile. In [15], an analytical subthreshold drain current model is presented based on drift-diffusion current using linear pocket profile.

In this paper, an analytical carrier conduction time delay model has been presented using the inversion layer charge density, surface potential and drift-diffusion based subthreshold drain current density model with the effective doping concentration based on the linear doping profiles for the pocket implanted nano scale n-MOSFET. The simulation is then carried out for different device and pocket profile parameters as well as bias conditions.

2. POCKET PROFILE MODEL

The pocket implanted n-MOSFET structure shown in Fig. 1 is considered in this work and assumed co-ordinate system is shown at the right side of the structure. Localized extra dopings are shown by circles near the source and drain sides. All the device dimensions are measured from the oxide-silicon interface. In the structure, the junction depth (r_j) is 25 nm. The oxide thickness (t_{ox}) is 3.0 nm, and it is SiO_2 with fixed oxide charge density of 10^{11} cm^{-2}. Uniformly doped p-type Si substrate is used with doping concentration (N_{sub}) of 4.5×10^{17} cm^{-3} with pocket implantation both at the source and drain sides with peak pocket doping concentration (N_{pm}) of 2.5×10^{18} cm^{-3} and pocket lengths (L_p) from 20 to 30 nm and source or drain doping concentration (N_{sd}) of 9.0×10^{20} cm^{-3}.

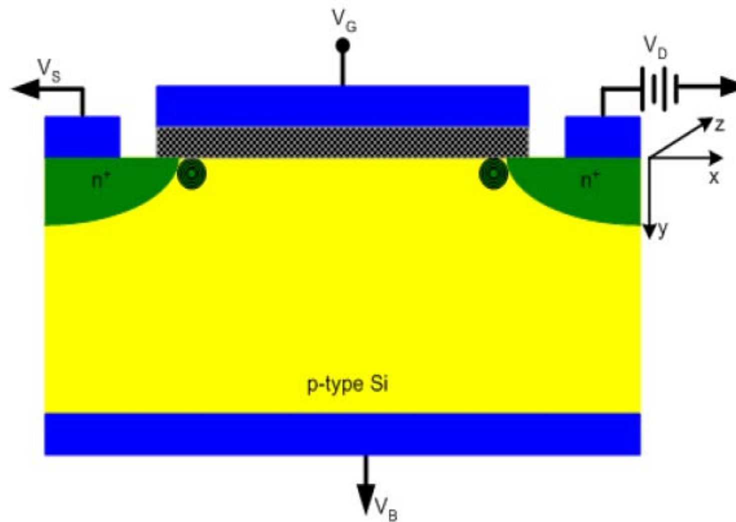

Fig. 1 Pocket Implanted n-MOSFET Structure

It has already been observed that by introducing Reverse Short Channel Effect (RSCE), Short Channel Effect (SCE) can be minimized [16]. This effect comes from the extra doping or pockets or fixed oxide charge located near the source and drain sides. Pocket implantation is done by adding extra impurity atoms (similar to that of the substrate) near the source and drain sides and the doping concentration decreases towards the centre of the device along the channel. In [17], few simulated lateral pocket doping profiles are provided for different channel lengths. After examining these pocket doping profiles, it is assumed that the pocket profiles to be linear and symmetric. It has been already shown that the linear profile can produce RSCE in threshold voltage model [18]. This profile assumes that the peak of the pocket doping concentration (N_{pm}) decreases linearly up to the substrate level concentration (N_{sub}) with pocket lengths (L_p) from both edges towards the center of the device as shown in Figs. 2-3.

At the source side, the pocket profile is given as

$$N_s(x) = N_{sub}\frac{x}{L_p} + N_{pm}\left(1 - \frac{1}{L_p}x\right) \tag{1}$$

At the drain side, the pocket profile is given as

$$N_d\left(x\right) = N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p}x\right) + N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p}x\right) \tag{2}$$

,where *x* represents the distance across the channel.

These two conceptual pocket profiles of equations (1) and (2) are integrated mathematically along the channel from the source side to the drain side and then the integration result is divided by the channel length (L) to derive an average effective doping concentration (N_{eff}) as in equation (3).

$$N_{eff} = N_{sub}\left(1 - \frac{L_p}{L}\right) + \frac{N_{pm}L_p}{L} \tag{3}$$

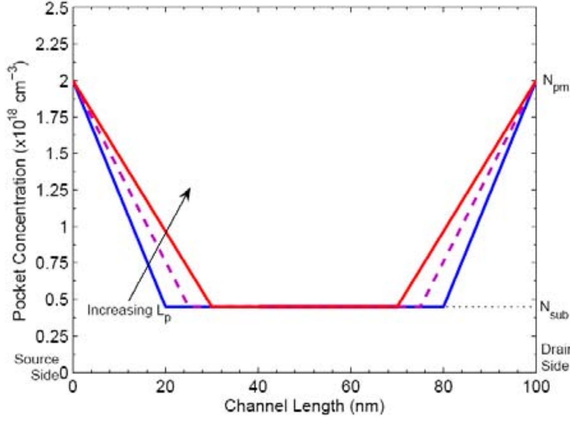

Fig. 2 Simulated pocket profiles at the surface for different pocket lengths, L_p = 20, 25 and 30 nm with peak pocket doping concentration, $N_{pm} = 2.0\times10^{18}$ cm^{-3}

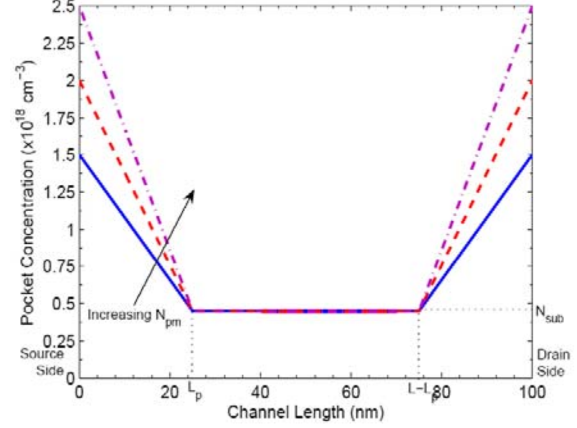

Fig. 3 Simulated pocket profiles at the surface for various peak pocket doping concentrations, $N_{pm} = 1.5\times10^{18}$, 2×10^{18} and 2.5×10^{18} cm^{-3} with pocket length, L_p = 25 nm

This effective doping concentration expression has been used in deriving the inversion layer charge density and subthreshold drain current density model using the drift-diffusion expression. Hence carrier conduction time delay has been derived. When $L_p << L$ for long channel device then the pocket profile has very little effect on uniform substrate concentration, but when L_p is comparable with L then the pocket profile parameters affects the substrate doping concentration at the surface of the n-MOSFET. This causes the different operational parameters, such as, surface potential, threshold voltage, subthreshold drain current etc. to change due to RSCE.

3. ANALYTICAL MODEL OF CONDUCTION TIME DELAY

In the subthreshold regime, the n-MOSFET is in weak inversion or diffusion mode, in which the electrons have to cross a potential barrier in the pocket doped silicon channel region. Based on the drift-diffusion equation, the electron current density, J_n in an n-MOSFET can be written as in equation (4).

$$J_n = q\left(-n\mu_n\frac{d\psi_s}{dx} + D_n\frac{dn}{dx}\right) = qD_n\left(\frac{-n}{\phi_{th}}\frac{d\psi_s}{dx} + \frac{dn}{dx}\right) \tag{4}$$

,where $\psi_s(x)$, n, D_n and q are surface potential, electron density, diffusion co-efficient and electronic charge respectively. ϕ_{th} is the thermal voltage given by equation (5).

$$\phi_{th} = \frac{kT}{q} = \frac{D_n}{\mu_{n,eff}} \tag{5}$$

Multiplying equation (4) by an integrating factor of $e^{-\psi_s/\phi_{th}}$, the right hand side of equation (4) can

be transformed into an exact derivative. Thus the electron current density equation (6) is found.

$$J_n = -qD_n N_{eff} \exp\left(-\frac{\varphi_{bi} - V_{BS}}{\phi_{th}}\right) \frac{\left(1 - \exp\left(\frac{V_{DS}}{\phi_{th}}\right)\right)}{\int_0^L \exp\left(-\frac{\psi_s}{\phi_{th}}\right) dx} \tag{6}$$

The complete analytical expression for the surface potential is used from [19] and is given in equation (7).

$$\psi_s(x) = \frac{c_1}{\sinh\sqrt{\frac{a_0}{a_2}}L} \sinh\sqrt{\frac{a_0}{a_2}}(L-x) + \frac{c_1 + V_{DS}}{\sinh\sqrt{\frac{a_0}{a_2}}L} \sinh\sqrt{\frac{a_0}{a_2}}x - \frac{b_1}{a_0} \tag{7}$$

,where the parameters a_0, a_2, b_1 and c_1 are given by:

$$a_0 = \frac{\varepsilon_{ox}}{t_{ox}}; \qquad a_2 = \frac{\varepsilon_s}{\eta} X_D$$

$$b_1 = qN_{eff} X_D - \frac{\varepsilon_{ox}}{t_{ox}}\left(V_{GS} - V_{BS} - V_{FB}\right)$$

$$c_1 = \varphi_{bi} - V_{BS} + \frac{b_1}{a_0}$$

The integral in the denominator of the right hand side of equation (6) is evaluated using the numerical integration technique. The diffusion co-efficient for electron (D_n) in equation (6) has been evaluated by using the Einstein relation given in equation (5) and the effective electron mobility ($_{n,eff}$) is obtained from [20] that also incorporates the inversion layer charges per unit area (Q_{inv}), which is given by equation (8).

$$Q_{inv} = C_{ox}\left(V_{gs} - V_{th}\right) + \sqrt{2q\varepsilon_{Si} N_{eff}\left(2\varphi_F + \psi_s\right)} \tag{8}$$

,where C_{ox}, V_{gs} and V_{th} are the oxide capacitance per unit area, gate to source voltage and threshold voltage respectively. V_{th} for the pocket implanted n-MOSFET is obtained from [18]. Since inversion layer charge is position dependent, it is calculated at different position of the channel from the source end to the drain end by using the surface potential model given in equation (7).

Using equations (6), (7) and (8), the carrier conduction time delay ($_{cd}$) model of inversion layer electrons can be obtained from the definition of the current density, and it is given by equation (9).

$$\tau_{cd} = \frac{|Q_{inv}|}{J_n} \tag{9}$$

4. RESULTS AND DISCUSSIONS

Simulation results are presented for the conduction time delay variations for different pocket profile and device parameters as well as for various temperature and bias conditions. The gate bias is varied from 0 to 0.5 V for different cases. Figure 4 shows that as the gate bias increases conduction time delay decreases in the subthreshold region for a particular peak pocket doping concentration. But if the peak pocket doping concentration decreases, conduction time delay also decreases for a particular gate voltage in the subthreshold regime. Because, at lower gate bias, if number of carriers in the channel decreases due to the reduction of effective doping concentration then scattering decreases and hence conduction time delay also decreases as carries require less time to cross the channel. Similar results are observed for pocket length variation as shown in Fig. 5.

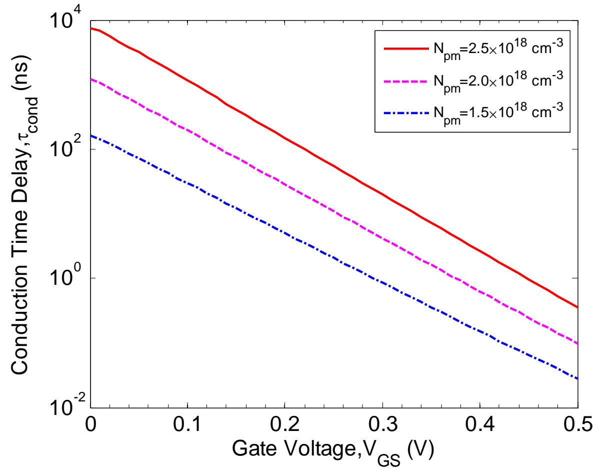

Fig. 4 Conduction time delay vs. gate voltage curves for various peak pocket doping concentration (N_{pm}) with channel length, L = 50 nm, pocket length, L_p = 25 nm, drain bias, V_{DS} = 0.05 V and substrate bias, V_{BS} = 0.0 V

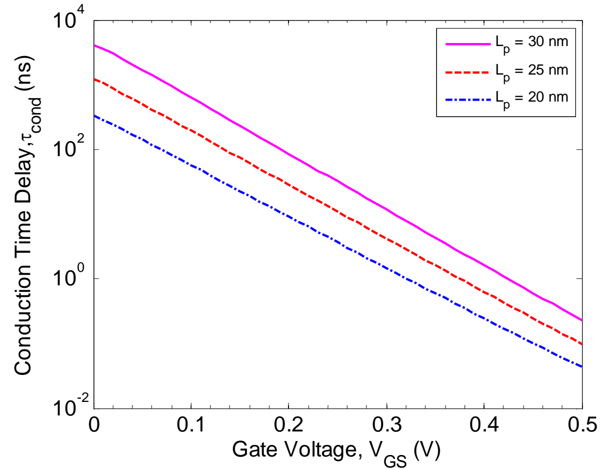

Fig. 5 Conduction time delay vs. gate voltage curves for various pocket lengths (L_p) with peak pocket doping concentration, N_{pm} = 2.0×10^{18} cm^{-3}, channel length, L = 50 nm, drain bias, V_{DS} = 0.05 V, substrate bias, V_{BS} = 0.0 V

Figure 6 shows the conduction time delay variations for different substrate doping concentrations. As the doping concentration is reduced for a particular gate bias, it is observed that the conduction time delay decreases slightly in the subthreshold regime due to the reduction of the Coulomb scattering processes in the channel and thus the carriers need less time to cross the channel. Figure 7 shows the conduction time delay variations for different oxide thicknesses. As the oxide thickness is reduced, it is observed that the conduction time delay decreases slightly in the subthreshold regime due to the greater control on the carriers in the channel.

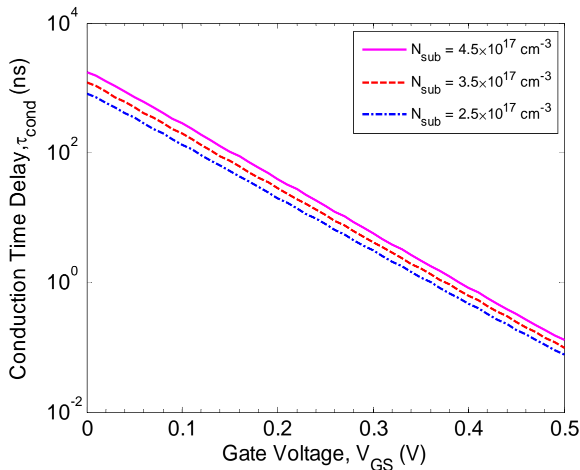

Fig. 6 Conduction time delay vs. gate voltage curves for various substrate doping concentration (N_{sub}) with L = 50 nm, N_{pm} = 2.0×10^{18} cm^{-3}, L_p = 25 nm, V_{DS} = 0.05 V, V_{BS} = 0.0 V

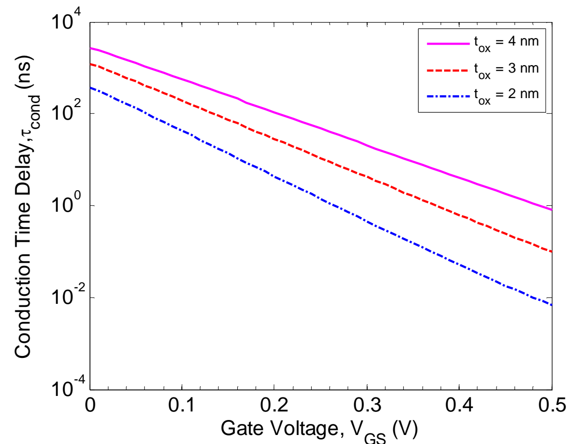

Fig. 7 Conduction time delay vs. gate voltage curves for various oxide thicknesses; N_{sub} = 3.5×10^{17} cm^{-3}, L = 50 nm, N_{pm} = 2.0×10^{18} cm^{-3}, L_p = 25 nm, V_{DS} = 0.05 V, V_{BS} = 0.0 V

Figure 8 shows the conduction time delay variations for different temperatures. As the temperature is reduced for a particular gate bias, it is observed that the conduction time delay

also reduces greatly in the subthreshold regime due to the reduction of the phonon scattering processes in the channel and thus the carriers require less time to cross the channel. Figure 9 shows the conduction time delay variations for different drain biases. As the drain bias is increased for a particular gate bias, it is observed that the conduction time delay decreases in the subthreshold regime due to the increment of the lateral electric field in the channel and thus the carriers require less time to cross the channel from the source side to the drain side.

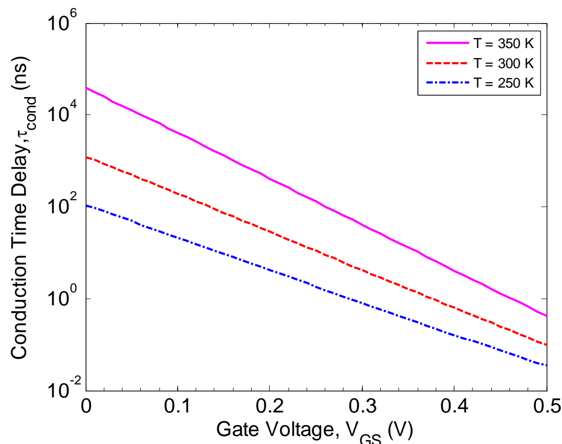

Fig. 8 Conduction time delay vs. gate voltage curves for various temperatures with N_{sub} = 3.5×10^{17} cm^{-3}, L = 50 nm, N_{pm} = 2.0×10^{18} cm^{-3}, L_p = 25 nm, V_{DS} = 0.05 V, V_{BS} = 0.0 V

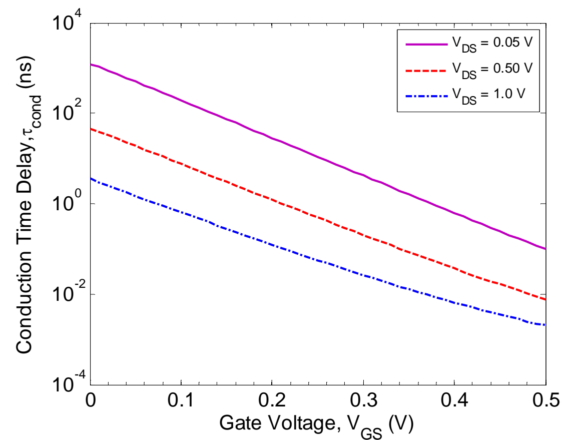

Fig. 9 Conduction time delay vs. gate voltage curves for various drain biases with N_{sub} = 3.5×10^{17} cm^{-3}, L = 50 nm, N_{pm} = 2.0×10^{18} cm^{-3}, L_p = 25 nm and V_{BS} = 0.0 V

Figure 10 shows the conduction time delay variations for different substrate biases. As the substrate bias is increased in the negative direction for a particular gate bias, it is observed that the conduction time delay increases in the subthreshold regime due to the increment of the inversion layer carriers in the channel and thus the carriers get scattered and require more time to pass the channel from the source side to the drain side.

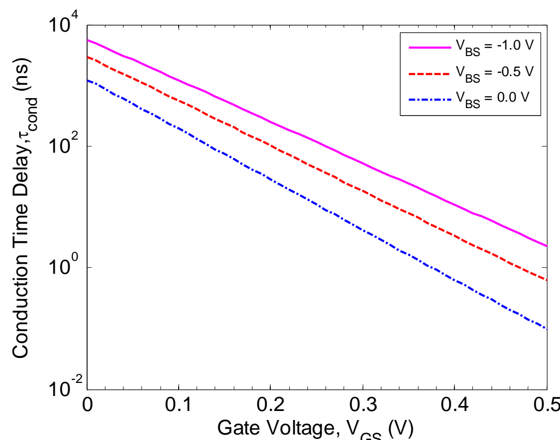

Fig. 10 Conduction time delay vs. gate voltage curves for various substrate biases with N_{sub} = 3.5×10^{17} cm^{-3}, L = 50 nm, N_{pm} = 2.0×10^{18} cm^{-3}, L_p = 25 nm, V_{DS} = 0.05 V

5. CONCLUSIONS

In this work, an analytical carrier conduction time delay model has been presented using the inversion layer charge density, surface potential and subthreshold drain current density models for the nano scale pocket implanted n-MOSFET. The model is developed by using two linear pocket doping profile models at the source and drain edges. The model includes the effective

doping concentration of these two linear pocket profiles. Electron current density is obtained from the conventional drift-diffusion equation. Then inversion channel charges per unit area are calculated for the pocket doped channel. The presented model is then studied by model simulations for different device and pocket profile parameters as well as bias conditions and temperatures. Simulation results reveal that the derived model predicts the conduction delay time very well. This type of pocket implanted n-MOSFET is advantageous over their bulk-silicon counterparts in nano scale regime. This work can further be extended for modeling the other parameters of this device structure.

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